LISTING OF CLAIMS:

1. (Currently Amended) A semiconductor wafer having an active surface, comprising:

a plurality of dice, each die having a plurality of contact pads formed on the active surface of the wafer;

a passivation layer disposed on said active surface, said passivation layer having a plurality of passivation layer vias formed therethrough and associated with at least a portion of said plurality of contact pads;

a resilient layer disposed on said passivation layer, said resilient layer having a plurality of resilient layer vias formed therethrough, wherein **all** sidewalls of at least some of said plurality of resilient layer vias are **fully** tapered **from the top to the bottom of said resilient layer** at ~~an~~ **substantially non-vertical** angle relative to the active surface of said wafer**, and wherein at least a portion of said plurality of passivation layer vias define a perimeter that completely encloses the perimeter of a corresponding resilient layer via**;

a plurality of under bump metallization stacks, each under bump metallization stack including a nickel-vanadium layer and a copper layer, wherein the nickel-vanadium layer is directly atop and in substantial contact with an associated contact pad and the copper layer is directly atop and in substantial contact with the nickel-vanadium layer, said under bump metallization stack being arranged such that at least some portion of the under bump metallization stack overlies a portion of said resilient layer; and

a plurality of solder bumps, each solder bump being formed on an associated under bump metallization stack.

2. (Previously Presented) The semiconductor wafer of claim 1, wherein said resilient layer comprises benzocyclobutene or a polyimide.

3. (Original) The semiconductor wafer of claim 1, wherein one or more of said plurality of under bump metallization stacks has a total thickness of less than about 15 kilo-angstroms.

4. (Original) The semiconductor wafer of claim 3, wherein one or more of said plurality of under bump metallization stacks has a total thickness of less than about 12 kilo-angstroms.

5. (Canceled)

6. (Currently Amended) The semiconductor wafer of claim 1 ~~5~~, wherein said passivation layer comprises a compound selected from the group consisting of silicon dioxide and silicon nitride.

7. (Canceled)

8. (Currently Amended) An integrated circuit device, comprising:

a plurality of contact pads formed on a first surface of said device;

a passivation layer disposed on said first surface, said passivation layer including a plurality of passivation layer vias formed therethrough and associated with at least a portion of said plurality of contact pads;

a resilient layer defining a substantially horizontal plane and disposed on said passivation layer, said resilient layer having a plurality of resilient layer vias formed therethrough and associated with at least a portion of said plurality of contact pads and at least a portion of said plurality of passivation layer vias, wherein one or more of said plurality of resilient layer vias

defines a primary axis extending therethrough and perpendicular to said substantially horizontal plane, and

contains one or more sidewalls that are **fully tapered from top to bottom such that no portion of sidewall is** ~~not~~ substantially parallel to said primary axis; and

a plurality of under bump metallization stacks, wherein one or more of said plurality of under bump metallization stacks each couple with an associated contact pad, and wherein each such under bump metallization stack comprises a plurality of metal or alloy layers, none of which are an aluminum layer, a titanium layer or a chromium layer,

wherein one or more of said plurality of passivation layer vias each define a perimeter that completely encloses the perimeter of a corresponding resilient layer via, such that an associated under bump metallization stack contacts said resilient layer but does not contact said passivation layer.

9. (Canceled)

10. (Original) The integrated circuit device of claim 8, wherein at least a portion of said plurality of under bump metallization stacks each comprise at least one layer selected from the group consisting of copper and nickel-vanadium.

11. (Original) The integrated circuit device of claim 10, wherein at least a portion of said plurality of under bump metallization stacks each comprise a copper layer directly atop and in substantial contact with a nickel-vanadium layer, which is in turn directly atop and in substantial contact with an associated contact pad.

12. (Original) The integrated circuit device of claim 8, wherein one or more of said plurality of under bump metallization stacks has a total thickness of less than about 15 kilo-angstroms.

13-14. (Canceled)

15. (Original) The integrated circuit device of claim 8, further comprising:

a plurality of solder bumps, wherein one or more of said plurality of solder bumps are each coupled with an associated under bump metallization stack and an associated contact pad.

16-20 (Canceled)

21. (Previously Presented) The integrated circuit device of claim 8, wherein said resilient layer completely covers all top and side surfaces of said passivation layer at at least a portion of said plurality of passivation layer vias.

22. (Previously Presented) The integrated circuit device of claim 8, wherein said passivation layer comprises a silicon based material.

23. (Previously Presented) The integrated circuit device of claim 22, wherein said passivation layer comprises one or more materials selected from the group consisting of SiO_2 and SiN.

24. (Previously Presented) The integrated circuit device of claim 8, wherein said resilient layer comprises benzocyclobutene or a polyimide.

25. (Currently Amended) An integrated circuit device, comprising:

a plurality of contact pads formed on an active surface of said device;

an inorganic passivation layer disposed upon said active surface, said passivation layer including a plurality of passivation layer vias formed therethrough and associated with at least a portion of said plurality of contact pads;

a polymeric resilient layer defining a substantially horizontal plane and disposed upon and substantially covering said passivation layer, said resilient layer having a plurality of resilient layer vias formed therethrough and associated with at least a portion of said plurality of

contact pads and at least a portion of said plurality of passivation layer vias, wherein one or more of said plurality of resilient layer vias defines a primary axis extending therethrough and perpendicular to said substantially horizontal plane, and contains one or more sidewalls that are **fully tapered from top to bottom such that no portion of sidewall is ~~not~~** substantially parallel to said primary axis;

a plurality of under bump metallization stacks, wherein one or more of said plurality of under bump metallization stacks each couple with an associated contact pad, and wherein each such under bump metallization stack comprises a plurality of metal or alloy layers, none of which are an aluminum layer, a titanium layer or a chromium layer, and wherein one or more of said plurality of passivation layer vias each define a perimeter that completely encloses the perimeter of a corresponding resilient layer via, such that an associated under bump metallization stack contacts said resilient layer but does not contact said passivation layer; and

a plurality of solder bumps, wherein one or more of said plurality of solder bumps are each coupled with an associated under bump metallization stack and an associated contact pad,

wherein one or more of said plurality of passivation layer vias each define a perimeter that completely encloses the perimeter of a corresponding resilient layer via, such that an associated under bump metallization stack contacts said resilient layer but does not contact said passivation layer.

26. (New) The integrated circuit device of claim 25, wherein said fully tapered sidewalls are tapered at an angle of about 45 degrees with respect to said substantially horizontal plane.

27. (New) The integrated circuit device of claim 8, wherein said fully tapered sidewalls are tapered at an angle of about 45 degrees with respect to said substantially horizontal plane.

28. (New) The semiconductor wafer of claim 1, wherein said fully tapered sidewalls are tapered at an angle of about 45 degrees with respect to said active surface of said wafer.